	EMERGING DISPLAY TECHNOLOGIES CORPORATION	FILE NO . CASS-006
		ISSUE : OCT . 11 , 1995
APPROVED BY: DATE		TOTAL PAGE : 17
Roger Yang		VERSION : 1

CUSTOMER ACCEPTANCE STANDARD SPECIFICATIONS

SPEC . NO . :

EU-SED1520D0A

FOR MESSRS :

CUSTOMER'S APPROVAL

DATE :

BY :

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EMERGING DISPLAY	MODEL NO. EU-SED1520D0A	VERSION 1
RECORDS OF REVISION	DOC. FIRST ISSUE OCT. 11, 1995	

DATE	REVISED DRAWING NO.	SUMMARY

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1. DESCRIPTION

The SED1520 is an LCD driver designed for use in a dot matrix LCD (Liquid Crystal Display) system capable of displaying characters and graphics . The bit-addressable display data which is sent from an 8-bit or 16-bit microcomputer is stored in a built-in display RAM which generates the signals required for driving the LCD . The circuitry has been designed to ensure a heretofore unavailable low power consumption and a wide range of operating voltages , thereby facilitating the construction of high-performance handheld small systems that run on batteries .

2. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATED VALUES	UNIT
SUPPLY VOLTAGE	V_{SS}	- 8.0 TO + 0.3	V
SUPPLY VOLTAGE	V_O	- 16.5 TO + 0.3	V
INPUT VOLTAGE	V_I	V_{SS} - 0.3 TO + 0.3	V

3. ELECTRICAL CHARACTERISTICS
3.1 DC CHARACTERISTICS

V_{DD} = 0 V Ta = - 20 TO 75°C

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
OPERATING VOLTAGE	VDD	—	2.4	—	6.0	V	
HIGH INPUT VOLTAGE	VIHT	—	VSS+2.0	—	VDD	V	1
	VIHC	—	0.2*VSS	—	VDD		
LOW INPUT VOLTAGE	VILT	—	VSS	—	VSS+0.8	V	1
	VILC	—	VSS	—	0.8*VSS		
HIGH OUTPUT VOLTAGE	VOHT	IOH = - 3.0 mA	VSS+2.4	—	—	V	2
	VOHC1	IOH = - 2.0 mA	VSS+2.4	—	—		
	VOHC2	IOH = - 120μA	0.2*VSS	—	—		
LOW OUTPUT VOLTAGE	VOLT	IOL = 3.0 mA	—	—	VSS+0.4	V	2
	VOLC1	IOL = 2.0 mA	—	—	VSS+0.4		
	VOLC2	IOL = 120μA	—	—	0.8*VSS		
INPUT LEAK CURRENT	ILI	—	-1.0	—	1.0	μA	3
OUTPUT LEAK CURRENT	ILO	—	-3.0	—	3.0	μA	4
STATIC CURRENT CONSUMPTION	IDDQ	$\overline{CS}$=CL=VDD	—	0.05	1.0	μA	
INPUT TERMINAL CAPACITY	CIN	Ta=25°C,f=1MHZ	—	5.0	8.0	PF	

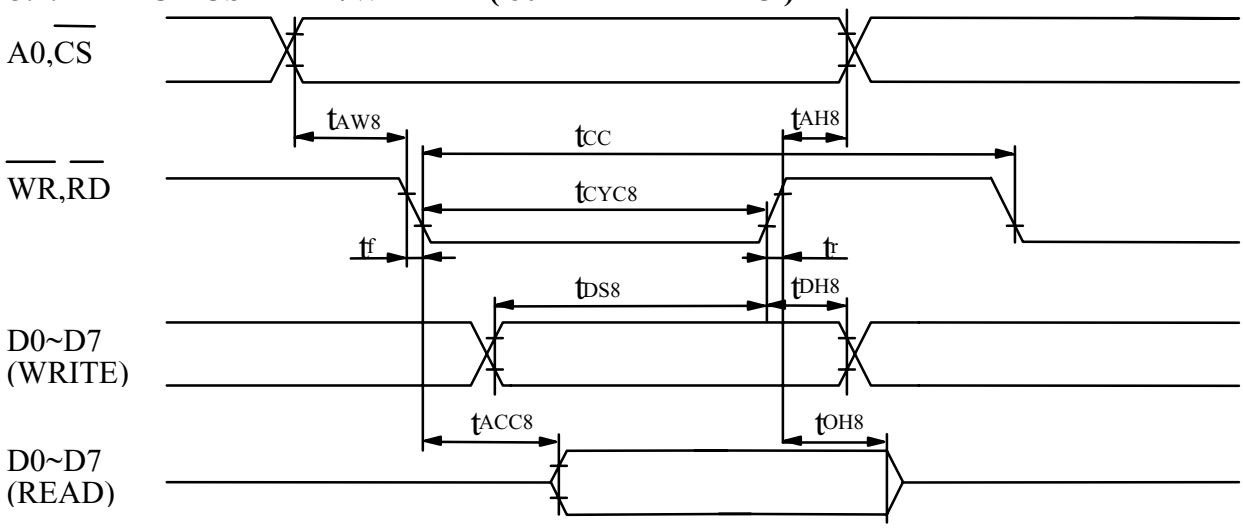
* 1 A wide range of operating voltages is guaranteed , except in case of abrupt voltage fluctuations during MPU access .

NOTE：

1. Pins D0 to D7,A0,E,R/$\overline{W}$,M/S,and,$\overline{CS}$,CL .$\overline{RES}$
2. Pins D0 to D7, $\overline{FR}$,and $\overline{OSC2}$.
3. Pins A0,E,R/$\overline{W}$,$\overline{CS}$,CL,$\overline{RES}$,M/$\overline{S}$.
4. Pins D0~D7,FR.

3.2 AC CHARACTERISTICS

3.2.1 MPU BUS READ/WRITE I (80 - FAMILY MPU)



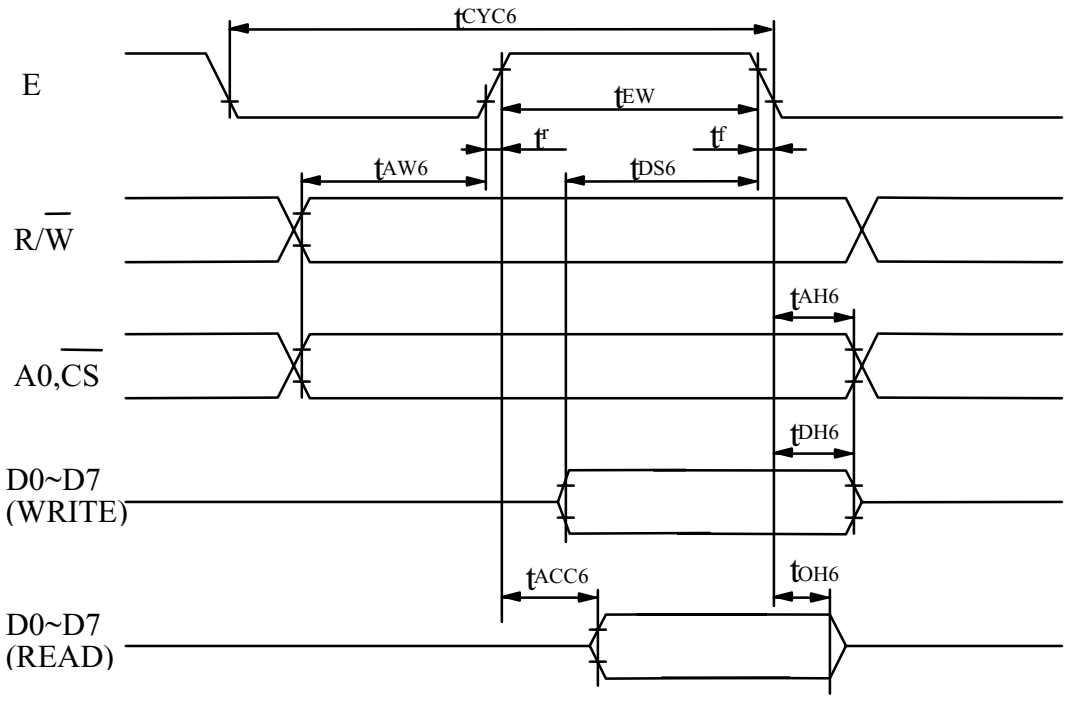
Ta = - 20 TO 75 deg . C , Vss = - 5.0 V±10% unless stated otherwise

PARAMETER	SIGNAL	SYMBOL	CONDITION	RATING		UNIT
			—	MIN	MAX	
ADDRESS HOLD TIME	A0,$\overline{CS}$	t_{AH8}	—	10	—	ns
ADDRESS SETUP TIME		t_{AW8}	—	20	—	ns
SYSTEM CYCLE TIME	$\overline{WR}$,$\overline{RD}$	t_{CYC8}	—	1000	—	ns
CONTROL PULSEWIDTH		t_{CC}	—	200	—	ns
DATA SETUP TIME	D0 TO D7	t_{DS8}	—	80	—	ns
DATA HOLD TIME		t_{DH8}	—	10	—	ns
$\overline{RD}$ ACCESS TIME		t_{ACC8}	CL = 1 0 0 P F	—	90	ns
OUTPUT DISABLE TIME		t_{CH8}		10	60	ns
RISE AND FALL TIME	—	t_r , t_f	—	—	15	ns

NOTE：

1. Increase parameter values by 200% when Vss = - 3.0 V .
2. All inputs must have a rise and fall time of less than 15 ns .

3.2.2 MPU BUS READ/WRITE Ⅱ (68-FAMILY MPU)



Ta = - 20 TO 75 deg . C , V_{SS} = - 5.0 V±10% unless stated otherwise

PARAMETER		SIGNAL	SYMBOL	CONDITION	RATING		UNIT
					MIN	MAX	
ADDRESS HOLD TIME		A0,$\overline{CS}$	t_{AH6}	—	10	—	ns
ADDRESS SETUP TIME		R/$\overline{W}$	t_{AW6}	—	20	—	ns
SYSTEM CYCLE TIME			t_{CYC6}	—	1000	—	ns
DATA SETUP TIME		D0 TO D7	t_{DS6}	—	80	—	ns
DATA HOLD TIME			t_{DH6}	—	10	—	ns
ACCESS TIME			t_{ACC6}	CL = 1 0 0 P F	—	90	ns
OUTPUT DISABLE TIME			t_{OH6}		10	60	ns
ENABLE PULSEWIDTH	READ	E	t_{EW}	—	100	—	ns
	WRITE			—	8	—	ns
RISE AND FALL TIME		—	t_r , t_f	—	—	15	ns

NOTE：

1. t_{CYC6} is the cycle time of $\overline{CS}$, E = H , not the cycle time of E .
2. Increase parameter values by 200% when Vss = - 3.0 V .
3. All inputs must have a rise and fall time of less than 15 ns .

4. RESET FUNCTION

Reset and interface configuration input . The driver is reset on any edge of $\overline{RES}$.
Initial parameter setup

- Display off
- Display start line register : line 1
- Static drive off
- Column address counter : 0
- Page address register : 3
- Duty : 1/32
- ADC : Forward (ADC : D0 = " 0 ")
- Read-modify-write off

In addition if the interface is configured by the level of $\overline{RES}$as given in the table below .

$\overline{RES}$	INTERFACE	A0	E	R/$\overline{W}$	$\overline{CS}$	D0 to D7
LOW	68 MPU	↑	↑	↑	↑	↑
HIGH	80 MPU	↑	$\overline{RD}$	$\overline{WR}$	↑	↑

5. FUNCTION DESCRIPTION

5.1 SYSTEM BUS DATA TRANSFER

The SED1520 drivers use the A0 , E (or $\overline{RD}$) and R/$\overline{W}$ (or $\overline{WR}$) signals to transfer data between the system MPU and internal registers . The combinations used are given in the table blow .

In order to match the timing requirements of the MPU with those of the display data RAM and control registers all data is latched into and out of the driver . This introduces a one cycle delay between a read request for data and the data arriving . For example when the MPU executes a read cycle to access display RAM the current contents of the latch are placed on the system data bus while the desired contents of the display RAM are moved into the latch . This means that a dummy read cycle has to be executed at the start of every series of reads . See Figure 1 .

No dummy cycle is required at the start of a series of writes as data is transferred automatically from the input latch to its destination .

COMMON	68 MPU	80 MPU		FUNCTION
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	READ DISPLAY DATA
1	0	1	0	WRITE DISPLAY DATA
0	1	0	1	READ STATUS
0	0	1	0	WRITE TO INTERNAL REGISTER (COMMAND)

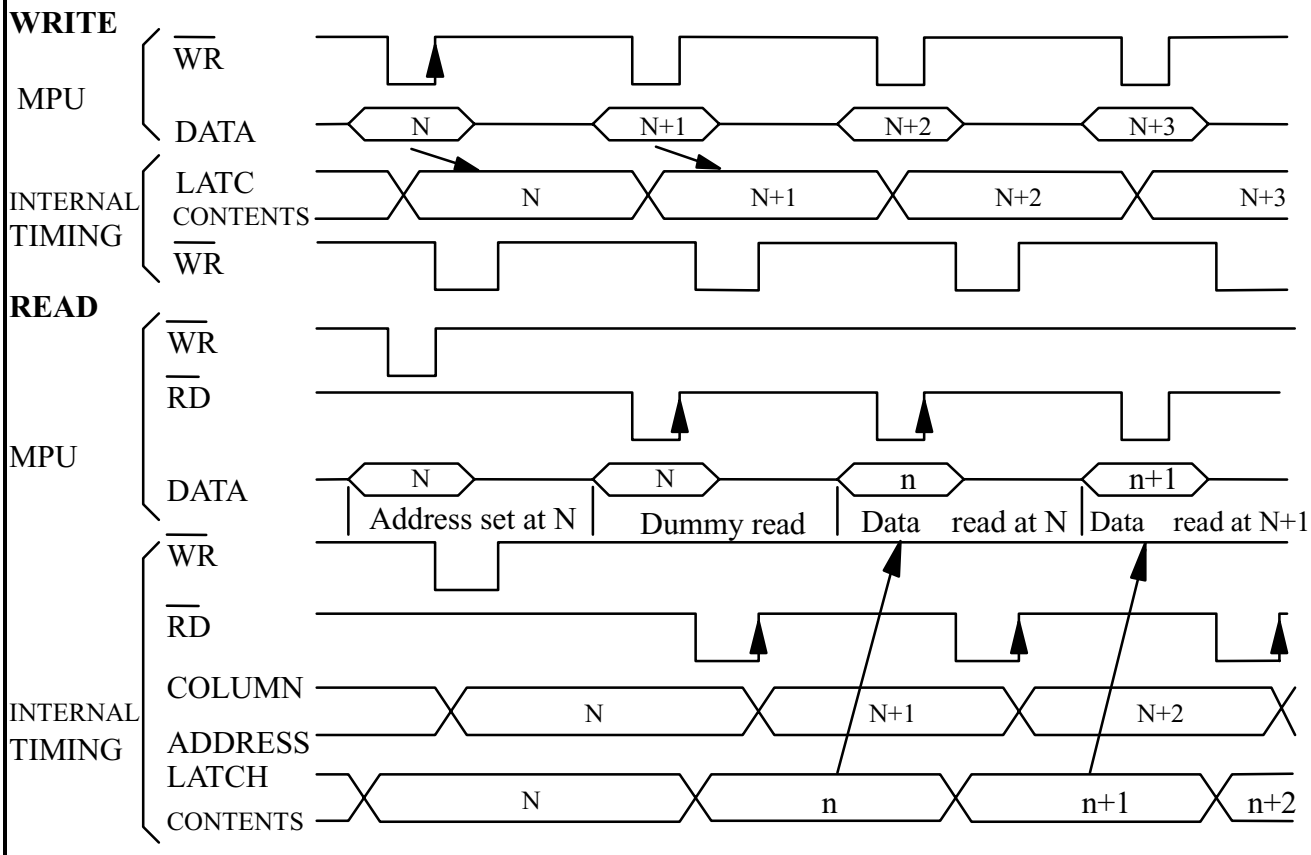


FIGURE 1 BUS BUFFER DELAY

5.2 DISPLAY START LINE AND LINE COUNT REGISTERS

The contents of this register form a pointer to a line of data in display data RAM corrsponding to the first line of the display (COM 0) , and are set by the Display Start Line command . Sec section 3 .
The contents of the display start line register are copied into the line count register at the atart of every frame , that is on each edge of FR . The line count register is incremented by the CL clock once for every display line , thus generating a pointer to the current line of data , in display data RAM , being transferred to the segment driver circuits .

5.3 COLUMN ADDRESS COUNTER

The column address counter is a 7-bit presettable counter that supplies the column address for MPU access to the display data RAM. See Figure 2 .The counter is incremented by one every time the driver receives a Read or Write Display Data command . Addresses above 50H are invalid , and the counter will not increment past this value . The contents of the column address counter are set with the Set Column Address command .

5.4 PAGE RESITER

The page resiter is a 2-bit register that supplies the page address for MPU access to the display data RAM . See Figure 2 .The contents of the page register are set by the Set Page Register command .

5.5 DISPLAY DATA RAM

The display data RAM stores the LCD display data . on a 1-bit per pixel basis . The relation-ship between display data , display address and the display is shown in Figure 2 .

6. INSTRUCTIONS DESCRIPTION

Table 1 lists the commands used with the SED1520. This LSI uses a combination of A0, $R/\overline{W}$ ($\overline{RD}$,$\overline{WR}$) to identify a data bus signal. Interpretation and execution of a command depends not on external clock but on internal timing alone. Therefore. a command can be executed so fast that no busy check is needed.

DETAILED DESCRIPTION OF COMMANDS

(1) DISPLAY ON/OFF

This command forces all display to turn on or off.

A0	E	$R/\overline{W}$	D7						D0
0	↓	0	1	0	1	0	1	1	D

D = 0 : Display OFF
D = 1 : Display ON

(2) DISPLAY START LINE

This command specifies a line address (shown in fig. 2) thus marking the display line that corresponds to COM0. Display begins with the specified line address and covers as many lines as match the display duty in address ascending order. Dynamic line address change with the Display Start Line command enables column-wise scrolling or page change.

A0	E	$R/\overline{W}$	D7						D0
0	↓	0	1	1	0	A4	A3	A2	A1	A0

Hight - order bits

A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0
0	0	0	0	1	1
		|			|
1	1	1	1	1	31

(3) SET PAGE ADDRESS

This command is used to specify a page address equivalent to a row address for MPU access to the display data RAM . A required bit of the display data RAM can be accessed by specifying its page address and column address . Changing the page address causes no change in display .

A0	E	$\overline{R/W}$	D7							D0
0	↓	0	1	0	1	1	1	0	A1	A0

A1	A0	PAGE
0	0	0
0	1	1
1	0	2
1	1	3

(4) SET COLUMN ADDRESS

This command specifies a display data RAM column address . The column address is incremented by 1 each time the MPU accesses from the set address to the display data RAM . thus it is possible for the MPU to gain continuous access to only the data . This incrementing stops with address 80 ; the page address is not continuously changed .

A0	E	$\overline{R/W}$	D7							D0
0	↓	0	0	A6	A5	A4	A3	A2	A1	A0

A6	A5	A4	A3	A2	A1	A0	COLUMN ADDRESS
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1
			|				|
1	0	0	1	1	1	1	79

(5) READ STATUS

A0	E	$\overline{R/W}$	D7							D0
0	↓	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : Busy being " 1 " means that system is performing an internal operation or is reset , no command is accepted before busy = " 0 " . As long as the cycle time requirement is met , no busy check is needed .

ADC : Indicates assignment of column addresses to segment drivers .
1 : normal , 0 : inverted

ON/OFF : Indicates display on or off
0 : DISPLAY ON
1 : DISPLAY OFF
This bit has polarity reverse to the display ON/OFF command .

RESET : Indicates that system is being initialized by the RES signal or the RESET command .
0 : DISPLAY MODE
1 : BEING RESET

(6) WRITE DISPLAY DATA

This command allows the MPU to write 8 bits of data into the display data RAM . Once the data is written , The column address is automatically incremented by 1 ; This enables the MPU to write multi-word data continuously .

A0	E	$\overline{R/W}$	D7							D0
1	↓	0	WRITE DATA							

(7) READ DISPLAY DATA

This command allows the MPU to read 8 bits of data from the display data RAM location specified by an column address and a page address . Once the data is read . the column address is automatically incremented by 1 ; this enables the MPU to read multi-word data continuously .

A dummy read is needed immediately after the column address is set .

A0	E	$\overline{R/W}$	D7 ——— D0
1	↓	1	READ DATA

(8) SELECT ADC

This command inverts the relation of assignment between display data RAM column addresses and segment driver outputs . In other words . the Select ADC command can software-invert the order of segment driver output pins , reducing the restrictions on the configuration of ICs at LCD module assembly . For details , see Fig . 2 .

Incrementing the column address by 1 , which takes place after the MPU writing or reading display data , follows the sequence of column addresses specified in Fig . 2 .

A0	E	$\overline{R/W}$	D7							D0
0	↓	0	1	0	1	0	0	0	0	D

D = 0 : Clockwise output (forward)
D = 1 : Counterclockwise output (reverse)

(9) STATIC DRIVE ON/OFF

This command forces all display to be on and , at the same time , all common output to be selected .

A0	E	$\overline{R/W}$	D7							D0
0	↓	0	1	0	1	0	0	1	0	D

D = 0 : Static drive off
D = 1 : Static drive on

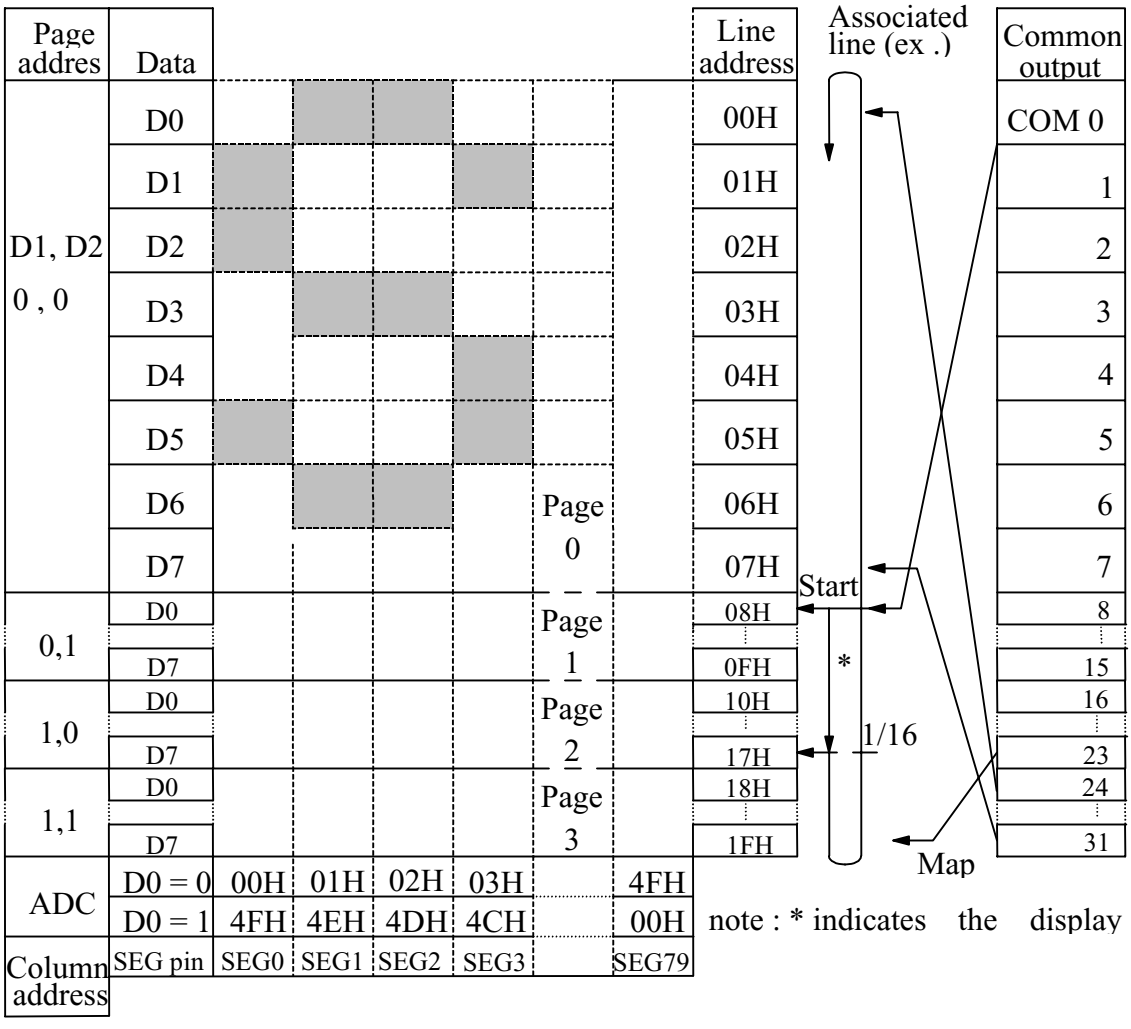


Figure 2 : Display Data RAM Addressing

(10) SELECT DUTY

This command is uesd to select the duty (degree of multiplexity) of LCD driving . It is valid for the SED1520F (actively operating LSI) only , not valid for the SED1521F (passively operating LSI) . The SED1521F operates with any duty determined by the FR signal .

A0	E	$\overline{R/W}$	D7						D0
0	↓	0	1	0	1	0	1	0	0	D

D = 0 : Duty 1/16

D = 1 : Duty 1/32

If the system contains both SED1520FOA (internal oscillation) and the SED1521FOA LSIs , they must have the same duty .

(11) READ MODIFY WRITE

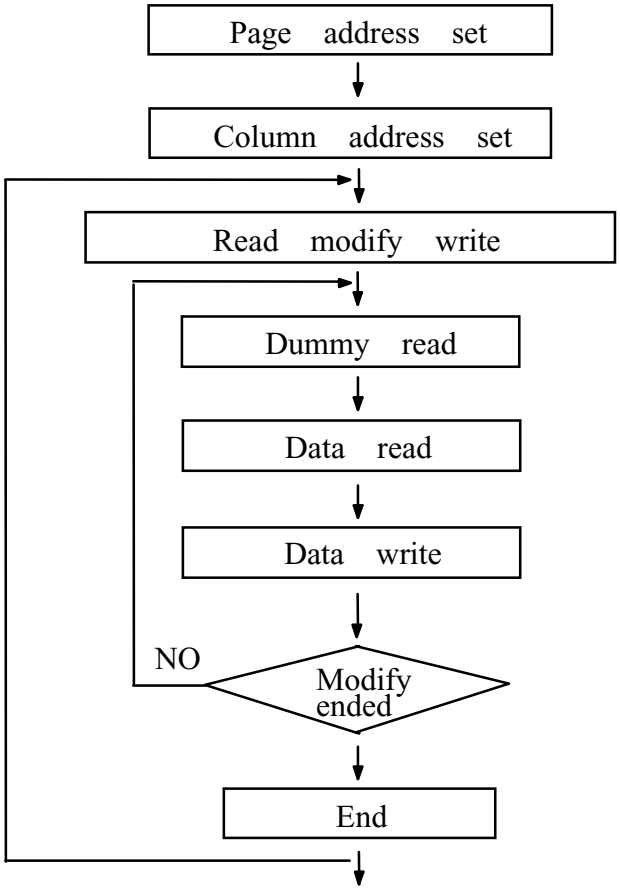
This command is used with the End command in a pair . Once it has been entered , the column address will be incremented not by the Read Display Data command but by the Write Display Data command only . This mode will stay until the End command is entered .

Entry of the End command causes the column address to return to the address which was valid when the Read Modify Write command was entered . This function lessens the load of the MPU when the data in a specific display area are repeatedly updated (as blinking cursor) .

A0	E	$\overline{R/W}$	D7							D0
0	↓	0	1	1	1	0	0	0	0	0

* . Even in the Read Modify Write mode , any command other than Read/Write Data can be used . However , the SET column address command cannot be used .

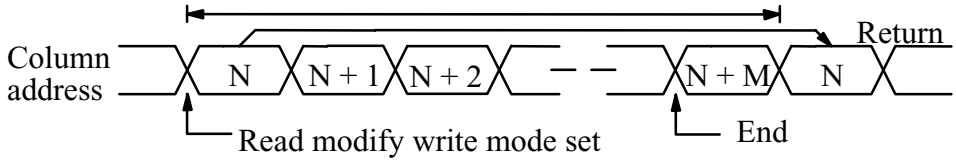
CURSOR BLINKING SEQUENCE



(12) END

This command cancels the Read Modify Write command , returning the column address to the initial mode address

A0	E	R/W	D7						D0
0	↓	0	1	1	1	0	1	1	0



(13) RESET

This command initializes the display start line register , column address counter , and set page address register to 3 page, It does not affect the . contents of the display data RAM .

For details .

The reset operation follows entry the Reset command .

A0	E	R/W	D7						D0
0	↓	0	1	1	1	0	0	0	1	0

Initialization at power- on is performed not by the Reset command but by a reset signal applied to the RES pin .

TABLE 1 COMMANDS

	COMMAND	CODE											FUNCTION
		A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0	
1	DISPLAY ON/OFF	0	↓	0	1	0	1	0	1	1	1	0/1	TURNS ALL DISPLAY ON OR OFF, INDEPENDENTLY OF DISPLAY RAM DATA OR INTERNAL STATUS . 1 : 0 : OFF (POWER-SAVING WITH STATIC DRIVE
2	DISPLAY START	0	↓	0	1	1	0	DISPLAY START ADDRESS (0-31)					SPECIFIES RAM LINE CORRESPONDING TO TOP LINE (COMO) OF DISPLAY .
3	SET PAGE ADDRESS	0	↓	0	1	0	1	1	1	0	PAGE (0-3)		SETS DISPLAY RAM PAGE IN PAGE ADDRESS REGISTER .
4	SET (SEGMENT) ADDRESS	0	↓	0	0	COLUMN ADDRESS (0 - 79)							SETS DISPLAY RAM COLUMN ADDRESS IN COLUMN ADDRESS REGISTER .
5	READ STATUS	0	↓	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0	READS THE STATUS: BUSY 1 : INTERNAL 0 : ADC 1 : CW OUTPUT 0 : CCW RESET 1 : BEING RESET 0 : NORMAL
6	WRITE DISPLAY DATA	1	↓	0	WRITE DATA								WRITES DATA FROM DATA INTO DISPLAY RAM. DISPLAY RAM LOCATION WHOSE ADDRESS HAS BEEN PRESET IS ACCESSED . AFTER ACCESS , THE COLUMN ADDRESS IS INCREMENTED BY 1.
7	READ DISPLAY DATA	1	↓	1	READ DATA								READS ATA FROM DISPLAY RAM ONTO DATA BU .
8	SELECT ADC	0	↓	0	1	0	1	0	0	0	0	0/1	USED TO INVERT RELATIONSHIP OF ASSIGNMENT BETWEEN DISPLAY RAM COLUMN ADDRESS AND SEGMENT DRIVER OUTPUTS . 0 : CW OUTPUT (FOWARD) 1 : CCW OUTPUT (REVERSE)

	COMMAND	CODE											FUNCTION
		A0	E	RW	D7	D6	D5	D4	D3	D2	D1	D0	
9	STATIC DRIVE ON/OF	0	↓	0	1	0	1	0	0	1	0	0/1	SELECTS NORMAL DISPLAY OR STATIC DRIVING OPERATION 1 : STATIC DRIVE (POWER-SAVING MODE) 0 : NORMAL DRIVING
10	SELECT DUTY	0	↓	0	1	0	1	0	1	0	0	0/1	SELECTS LCD CELL DRIVING DUTY . 1 : 1/32 0 : 1/16
11	READ MODIFY WRIT	0	↓	0	1	1	1	0	0	0	0	0	INCREMENTS COLUMN ADDRESS COUNTER BY 1 WHEN DISPLAY DATA IS WRITTEN . (THIS IS NOT DONE WHEN DATA IS
12	END	0	↓	0	1	1	1	0	1	1	1	0	CLEARS READ MODIFY WRITE MODE .
13	RESET	0	↓	0	1	1	1	0	0	0	1	0	SOFTWARE RESET

* WITH DISPLAY OFF COMMAND (1) , STATIC DRIVE GOING ON (9) INVOLKES POWER-SAVING MODE .