

	EMERGING DISPLAY TECHNOLOGIES CORPORATION	FILE NO . CASS-007
		ISSUE : NOV . 03 , 1995
APPROVED BY: DATE		TOTAL PAGE : 22
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CUSTOMER ACCEPTANCE STANDARD SPECIFICATIONS

SPEC . NO . :

EU - T 6 9 6 3 C

FOR MESSRS :

CUSTOMER'S APPROVAL

DATE :

BY :

EMERGING DISPLAY

MODEL NO . EU - T 6 9 6 3 C	VERSION 1
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RECORDS OF REVISION

DOC . FIRST ISSUE
NOV . 03 , 1995

DATE	REVISED DRAWING NO.	SUMMARY

TABLE OF CONTENTS

NO.	ITEM	PAGE
1.	DESCRIPTION -----	1
2.	ABSOLUTE MAXIMUM RATINGS -----	1
3.	ELECTRICAL CHARACTERISTICS -----	2 ~ 3
4.	FLOW CHART OF COMMUNICATIONS WITH MPU -----	4 ~ 6
5.	DESCRIPTION OF COMMAND -----	7 ~ 20
6.	COMMAND LIST -----	21
7.	CHARACTER CODE MAP -----	22

1. DESCRIPTION

T6963C is LCD controller designed to be used for control LCD driver LSIs and display data Memories .

It has an 8 bit parallel data bus and control lines for reading or writing through a MPU I/F . It to be directly connected TMPZ-80 .

It has 128 words character generator ROM with the capability to control external display RAM of up to 64K bytes . Allocation of text , graphics and external character generator RAM can be easily made and the display window can be freely moved within the allocated memory range .

It supports a very broad range of LCD formats by selecting different combinations on a set of programmable inputs . It can be used in text ,graphic and a combination of text and graphic modes and has various attribute functions .

2. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	TEST CONDITION	RATING	UNIT
SUPPLY VOLTAGE	VDD		- 0.3 TO +7.0	V
INPUT VOLTAGE	VIN		- 0.3 TO VDD +0.3	V
OPERATING TEMPERATURE	TOPR		- 10 TO +70	°C
STORAGE TEMPERATURE	TSTG		-55 TO +125	°C

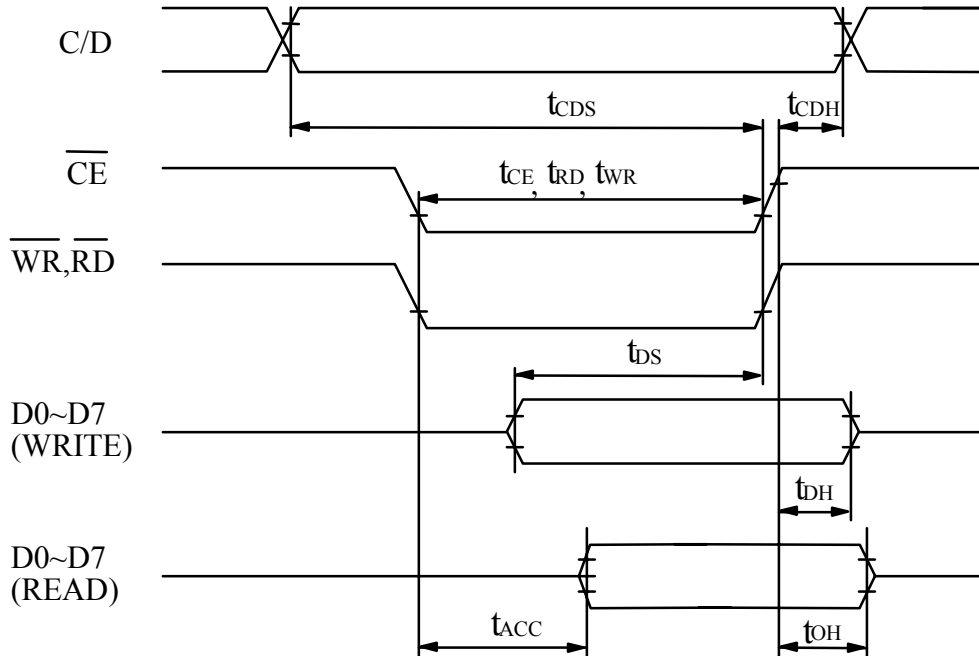
NOTE : VALUES MEASURED AT VSS = 0V.

3. ELECTRICAL CHARACTERISTICS**3.1 DC CHARACTERISTICS**

UNLESS OTHERWISE SPECIFIED , VSS = 0V , VDD = 5.0V±10% , Ta = 25 °C

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
OPERATING VOLTAGE	VDD	—	4.5	5.0	5.5	V
HIGH INPUT VOLTAGE	VIH	—	VDD-2.2	—	VDD	V
LOW INPUT VOLTAGE	VIL	—	0	—	0.8	V
HIGH OUTPUT VOLTAGE	VOH	—	VDD-0.3	—	VDD	V
LOW OUTPUT VOLTAGE	VOL	—	0	—	0.3	V
HIGH OUTPUT RESISTANCE	ROH	VOUT = VDD - 0.5 V	—	—	400	Ω
LOW OUTPUT RESISTANCE	ROL	VOUT = 0.5V	—	—	400	Ω
INPUT PULL UP RESISTANCE	RPU	—	50	100	200	KΩ
OPERATING FREQUENCY	FOSC	—	0.4	—	5.5	MHZ
CURRENT CONSUMPTION (HALT)	IDD (2)	VDD = 5.0 V	—	—	3	μA

3.2 AC CHARACTERISTICS

UNLESS OTHERWISE SPECIFIED, $V_{SS} = 0V$, $V_{DD} = 5.0V \pm 10\%$, $T_a = -10$ TO $+70$ °C

ITEM	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
C/D SET UP TIME	t_{CDS}	—	100	—	ns
C/D HOLD TIME	t_{CDH}	—	10	—	ns
CE, RD, WR PULSE WIDTH	t_{CE}, t_{RD}, t_{WR}	—	80	—	ns
DATA SET UP TIME	t_{DS}	—	80	—	ns
DATA HOLD TIME	t_{DH}	—	40	—	ns
ACCESS TIME	t_{ACC}	—	—	150	ns
OUTPUT HOLD TIME	t_{OH}	—	10	50	ns

4. FLOWCHART OF COMMUNICATIONS WITH MPU**4.1 STATUS READ**

Before sending data (read/write) , command it is necessary to check the status .

Status check

Status of T6963C can be read from data lines .

$\overline{\text{RD}}$	L
$\overline{\text{WR}}$	H
$\overline{\text{CE}}$	L
C/D	H
D0~D7	Status word

T6963C status word format is following .

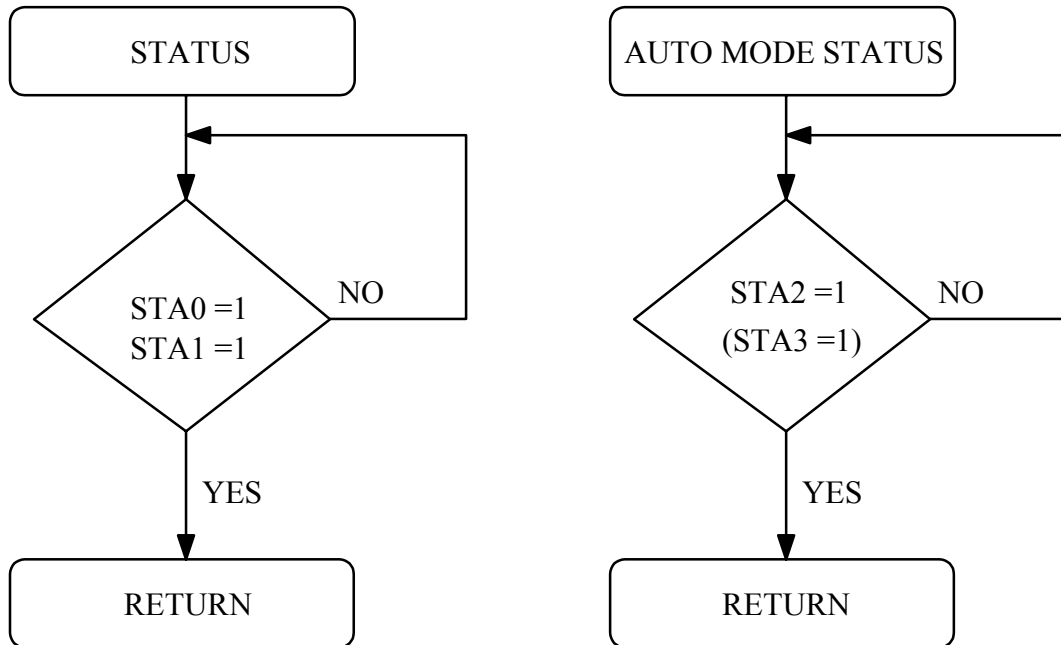
MSB						LSB	
STA7 D7	STA6 D6	STA5 D5	STA4 D4	STA3 D3	STA2 D2	STA1 D1	STA0 D0

STA0	Check capability of command execution	0 : Disable	1 : Enable
STA1	Check capability of data read/write	0 : Disable	1 : Enable
STA2	Check capability of auto mode data read	0 : Disable	1 : Enable
STA3	Check capability of auto mode data write	0 : Disable	1 : Enable
STA4	Not use		
STA5	Check capability of controller operation	0 : Disable	1 : Enable
STA6	Error flag . Using screen peek/copy command	0 : No error	1 : Error
STA7	Check the condition blink	0 : Display off	1 : Normal display

NOTE 1: It is necessary to check STA0 and STA1 at the same time . The error is happened by sending data at executing command .

NOTE 2: The status check will be enough to check STA0 / STA1 .

NOTE 3: STA2 / STA3 are valid in auto mode STA0 / STA1 are invalid .

Status checking flow

NOTE 4: It is impossible to save status check in the case of command of MSB0 .

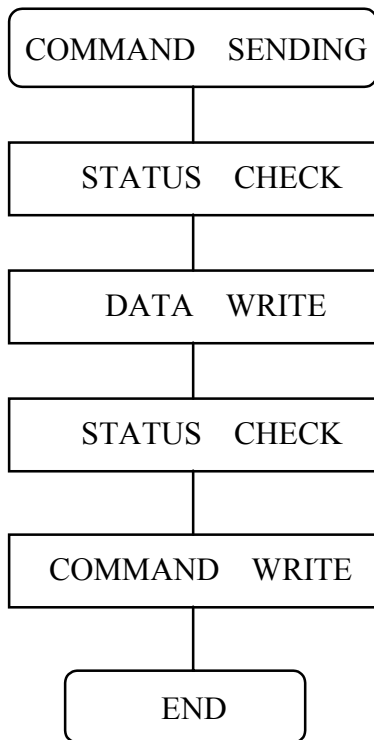
To have the delay time cannot be save status check . The interrupt of hardware is happened at the end of lines . If command of MSB0 is sent in this period ,the command executing is waited . The state of waiting doesn't be known without to check status . The sending next command or data is disregarded or rewrites data of waiting command .

4.2 DATA SET

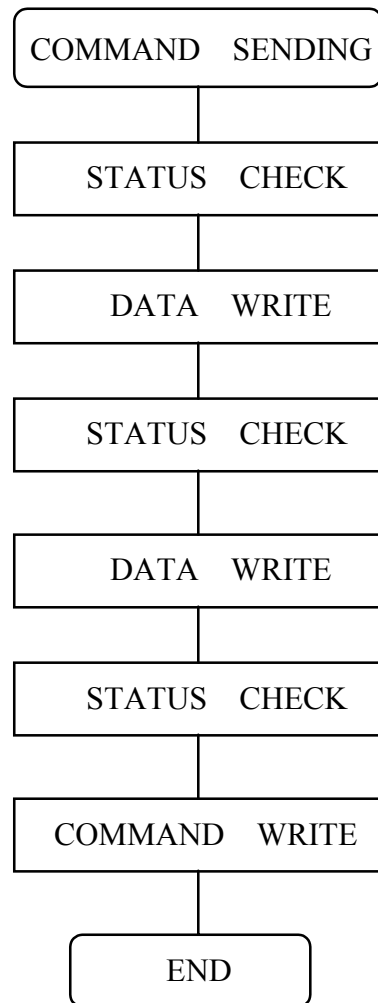
In T6963C , the data have been set and command executes .

The order of procedure of command sending

1 . THE CASE OF 1 DATA



2. THE CASE OF 2 DATA



NOTE : In case of over 2 data sending , the last data (or last 2 data) is valid .

5. DESCRIPTION OF COMMAND**5.1 REGISTER SET**

CODE	HEX	FUNCTION	D1	D2
00100001	21H	CURSOR POINTER SET	X ADRS	Y ADRS
00100010	22H	OFFSET REGISTER SET	DATA	00H
00100100	24H	ADDRESS POINTER SET	LOW ADRS	HIGH ADRS

5.1.1 CURSOR POINTER SET

The position of cursor is specified by X ADRS , Y ADRS . The cursor position is moved only by this command .The cursor pointer doesn't have the function of increment and decrement .The shift of cursor are set by this command .X ADRS , Y ADRS are specified following .

X ADRS 00H~4FH (Lower 7bits are valid)

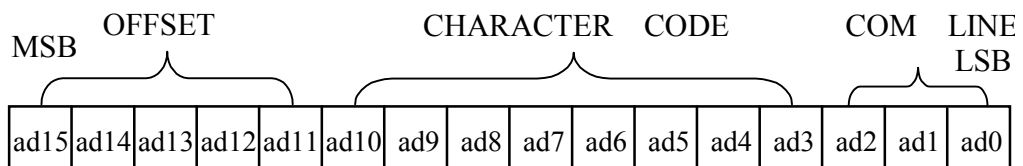
Y ADRS 00H~1FH (Lower 5bits are valid)

X ADRS 00~4FH

Y ADRS 00~0FH

5.1.2 OFFSET REGISTER SET

The offset register is used to determine external character generator RAM area . T6963C has 16 bit address lines as follow .



The upper 5 bit (ad15~ad11) are determined by offset register .The middle 8 bit (ad10~ad3) are determined by character code .The lower 3 bit (ad2~ad0) are determined by vertical counter .The lower 5 bit of D1 (data) are valid .

The data format of external character generator RAM .

MODEL NO. EU - T 6 9 6 3 C	VERSION 1	PAGE 8
-------------------------------	--------------	-----------

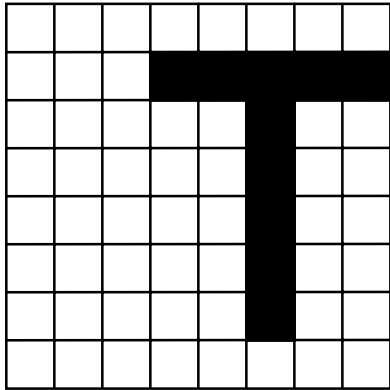
The relationship of display RAM address and offset register

DATA OF OFFSET REGISTER CG RAM HEX ADDRESS (START - END)

00000	0000 - 07FFH
00001	0800 - 0FFFH
00010	1000 - 17FFH
11100	E000 - E7FFH
11101	E800 - EFFFH
11110	F000 - F7FFH
11111	F800 - FFFFH

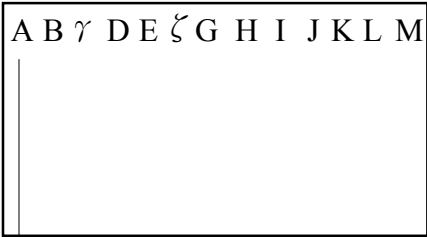
(EXAMPLE 1)

OFFSET REGISTER	02H				
CHARACTER CODE	80H				
CHARACTER GENERATOR RAM START ADDRESS	0001	0100	0000	0000	
	1	4	0	0H	

	(ADDRESS)	(DATA)
	1400H	00H
	1400H	1FH
	1400H	04H
	1400H	04H
	1400H	04H
	1400H	04H
	1400H	04H
	1400H	04H
	1400H	00H

(EXAMPLE 2)

The relationship of display RAM data and display character

	(RAM DATA)	(CHARACTER)
	21H	A
	22H	B
	83H	γ
	24H	D
	25H	E
	86H	ζ

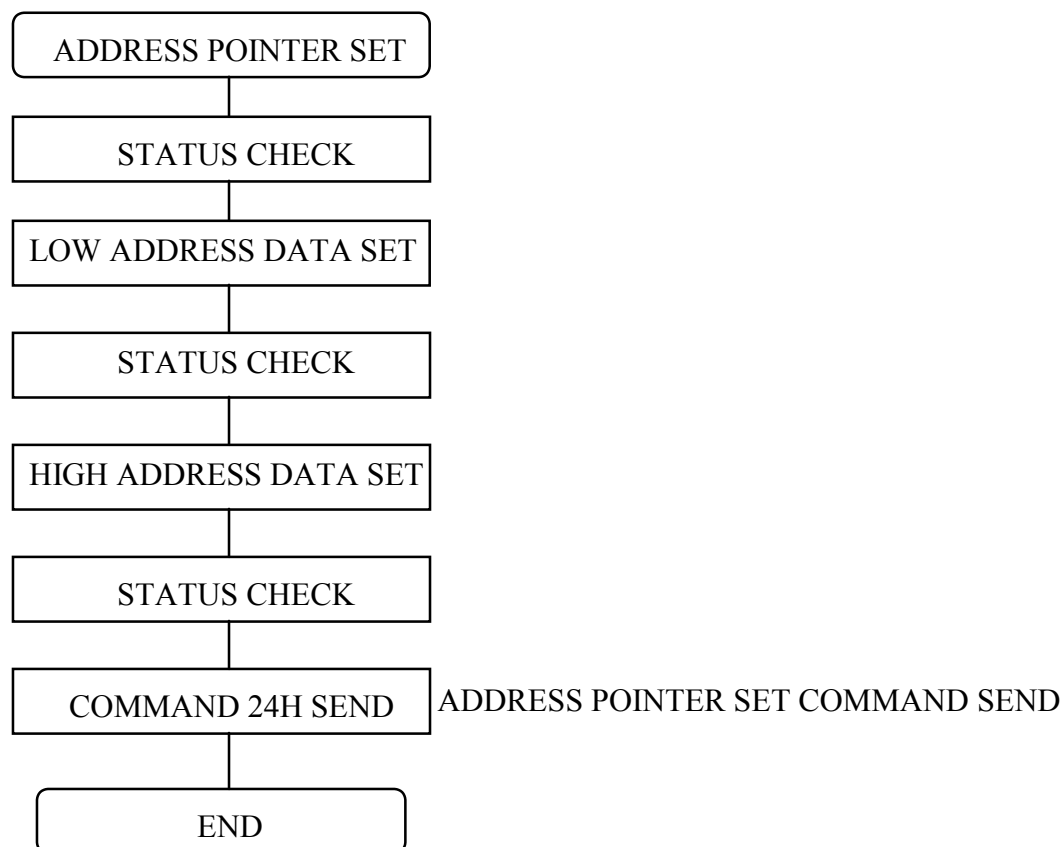
DISPLAY CHARACTER

γ and ζ are displayed by character generator RAM .

5.1.3 ADDRESS POINTER SET

The address pointer set command is used to indicate the start address for writing (or reading) to external RAM .

The flow chart address pointer set command

**5.2 CONTROL WORD SET**

CODE	HEX	FUNCTION	D1	D2
01000000	40H	TEXT HOME ADDRESS SET	LOW ADDRESS	HIGH ADDRESS
01000001	41H	TEXT AREA SET	COLUMNS	00H
01000010	42H	GRAPHIC HOME ADDRESS SET	LOW ADDRESS	HIGH ADDRESS
01000011	43H	GRAPHIC AREA SET	COLUMNS	00H

The home address and column size are defined by this command .

5.2.1 TEXT HOME ADDRESS SET

The starting address of external display RAM for Text display is defined by this command , The text home address shows the left end and most upper position .

The relationship of external display RAM address and display position

TH		TH+CL
TH+TA		TH+TA+CL
(TH+TA)+TA		TH+2TA+CL
(TH+2TA)+TA		TH+3TA+CL
TH+(n-1)TA		TH+(n-1)TA+CL

TH : Text home address

TA : Text area number (columns)

CL : Columns are fixed by hardware . (pin - programmable)

(EXAMPLE)

Text home address : 0000H

Text area : 0020H

0000H	0001H		001EH	001FH
0020H	0021H		003EH	003FH
0040H	0041H		005EH	005FH
0060H	0061H		007EH	007FH

5.2.2 GRAPHIC HOME ADDRESS SET

The starting address of external display RAM for Graphic display is defined by this command . The graphic home address shows the left end most upper line .

The relationship of external display RAM address and display position

GH		GH+CL
GH+GA		GH+GA+CL
(GH+GA)+GA		GH+2GA+CL
(GH+2GA)+GA		GH+3GA+CL
GH+(n-1)GA		GH+(n-1)GA+CL

GH : Graphic home address

GA : Graphic area number (columns)

CL : Columns are fixed by hardware . (pin - programmable)

(EXAMPLE)

Graphic home address : 0000H

Graphic area : 0020H

0000H	0001H		001EH	001FH
0020H	0021H		003EH	003FH
0040H	0041H		005EH	005FH
0060H	0061H		007EH	007FH
0080H	0081H		009EH	009FH
00A0H	00A1H		00BEH	00BFH
00C0H	00C1H		01DEH	01DFH
00E0H	00E1H		01FEH	01FFH
0100H	0101H		011EH	011FH
0120H	0121H		013EH	013FH
0140H	0141H		015EH	015FH
0160H	0161H		017EH	017FH
0180H	0181H		019EH	019FH
01A0H	01A1H		01BEH	01BFH
01C0H	01C1H		01DEH	01DFH
01E0H	01E1H		01FEH	01FFH

5.2.3 TEXT AREA SET

The columns of display are defined by the hardware setting . This command can be used to adjust columns of display .

(EXAMPLE)

LCD size : 20 columns , 4 lines

Text home address : 0000H

Text area : 0014H

0000	0001	-----	0013	0014	-----	001F
0014	0015	-----	0027	0028	-----	0033
0028	0029	-----	003B	003C	-----	0047
003C	003D	-----	004F	0050	-----	005B



5.2.4 GRAPHIC AREA SET

The columns of display are defined by the hardware setting . This command can be used to adjust columns of graphic display .

(EXAMPLE)

LCD size : 20 columns , 4 lines

Text home address : 0000H

Text area : 0014H

0000	0001	-----	0013	0014	-----	001F
0014	0015	-----	0027	0028	-----	0033
0028	0029	-----	003B	003C	-----	0047
003C	003D	-----	004F	0050	-----	005B
0050	0051	-----	0063	0064	-----	006F
0064	0065	-----	0077	0078	-----	0083
0078	0079	-----	008B	008C	-----	0097
008C	008D	-----	009F	00A0	-----	00AB
00A0	00A1	-----	00B3	00B4	-----	00BF
00B4	00B5	-----	00C7	00C8	-----	00D3
00C8	00C9	-----	00DB	00DC	-----	00E7
00DC	00DD	-----	00EF	00F0	-----	00FD
00F0	00F1	-----	0103	0104	-----	011F
0104	0105	-----	0127	0128	-----	0123
0128	0129	-----	013B	013C	-----	0147
013C	013D	-----	014F	0150	-----	015B



The address in graphic area can be continuous and RAM area can be used without ineffective area , if graphic area is defined the same number as the actual column number of LCD display .